**PFC Software design Document (AC to DC converter)**

# Plant model

The overview of a Totem pole interleaved PFC AC-DC converter consists of 3 inductors connected to a high frequency half bridge, and their combined output connected to a low frequency for synchronous rectification. The system also consists of line voltage sensing, line current sensing, inductor current sensing, output voltage sensing, a MCU for control, and gate drivers to drive the FETs. The chosen MCU for the application is the Texas instruments [F28069m](https://www.ti.com/tool/LAUNCHXL-F28069M?utm_source=google&utm_medium=cpc&utm_campaign=epd-c2x-null-prodfolderdynamic-cpc-pf-google-wwe&utm_content=prodfolddynamic&ds_k=DYNAMIC+SEARCH+ADS&DCM=yes&gclid=Cj0KCQjw3v6SBhCsARIsACyrRAklrhDMmNKasowDrrIfKbNlJ5QYCcJ0WlZR8FNb1obrrISz5O3HVjYaAve4EALw_wcB&gclsrc=aw.ds) launch pad.

Diagram, schematic

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Figure 1.1: System overview showing PFC architecture, MCU, gate driver, FETs, current and voltage sense

## switching model SIMULINK

Below is a simplified switching model of the interleaved PFC with a single stage of the interleaved stack and diodes used to represent the low frequency switches to the right of the model, the high frequency switches on the left used to modulate current and subsequently voltage interchangeably depending on the cycle of the AC input, ie: positive or negative half cycle

Diagram, schematic

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Figure 1.2: simplified model of a single-phase PFC showing the configuration of the inductor, high frequency switches, rectification diodes and output capacitance

## average model Simulink

### Positive half cycle of AC signal

A picture containing diagram

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Figure 1.3: Derivation of the system dynamic equation during the positive half cycle

Diagram

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Fig 1.4: Simulink representation of the system dynamic equations during the positive half cycle

### Negative half cycle of AC signal

Diagram

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Figure 5: Derivation of the system dynamic equation during the negative half cycle

Fig 1.5: Simulink representation of the system dynamic equations during the positive half cycle

Diagram

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Fig 1.6: Simulink representation of the system dynamic equations during the Negative half cycle

## transfer function

### Inner Current loop Transfer function

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### Outer Voltage loop Transfer function

Text

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# Closed loop current Controller

## Current control Architechture

Inductor current reference reference

PWM duty cycle

PI controller

Inductor current measurement

Power reference

AC rectification of current reference

Figure 2.1: Control loop for current controller

## 100 khz interrupt service routine for current controller

## PI Controller gain

Proportional gain: 0.027

Integral gain: 140

## Feedback gains

AC Voltage gain: to scale the AV voltage input back to 400v from the 0-3 of the ADC : 230.79

Inductor current gain for inductor current 1, 2 & 3 that represent the 3 stages of the interleaved: 40

## Feed forward gains

### Power reference

(2\*output\_power)/maximum\_VAC

Maximum\_VAC = 400

Output\_power = 5000

### AC rectification of current reference

1/maximum\_VAC

The AC voltage which ranges from Vm to -Vm (maximum line voltage) is normalized by subtracting the VAC\_N (negative line voltage measurement) from VAC\_P (positive line voltage measurement) and divided by the Vm to get a reference ac voltage of -1 to 1.

# Closed loop Voltage controller

## Voltage control block

PI Controller

Voltage reference error signal Inductor current reference

Voltage feedback

Figure 3.1: Control loop for voltage controller

## 10kz interrupt service routine for current controller

## Controller gains

Proportional control gain: 0.03

Integral Controller gain: 0.4

## Feedback gains

DC bus voltage gain: required to convert the DC voltage measurement from 0 -3v to the DC bus voltage measurement is 307.39

# Soft switch

During zero crossing of the of the AC input, the controller switches the high frequency driving FET from the bottom left (in figure 2) one for positive half cycle to the top left FET to enable CCM. Hence the controller resets and there is a current spike consistent with the overshoot expected at the beginning of the signal cycle. To circumvent that a soft switch algorithm is implemented which disables both low frequency switches and ramps up the duty cycle of the FET required for CCM in that cycle (positive or negative half cycle).

Diagram

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Figure 4.1: PWM Sequence With Soft Starting to Reduce Current Spike at Zero-Crossing

Chart, line chart

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Figure 4.2: Current output without the implementation of soft-start

Line chart

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Figure 4.3: Current output with the implementation of soft-start

# Filters

## Inductor current Filter

Low pass filter to remove high frequency noise at 100 khz : design second order low pass filter with cut-off frequency at 50 khz

Graphical user interface

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Figure 5.1: 50 khz generated low pass filter frequency response

## AC voltage Filter

Low pass filter to remove high frequency noise at 100 khz-design second order low pass filter with cut-off frequency at 50 khz

## DC bus voltage filter

Notch filter to remove couple AC noise in the 110 to 130Hz range

Graphical user interface, application

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Fig: 5.2: 2nd order Chebyshev notch filter 110 -130 Hz frequency response

## AC CURRENT FILTER

Low pass filter to remove high frequency noise at 100 khz-design second order low pass filter with cut-off frequency at 50 khz.

## Temperature sense filter

Low pass filter 1kz to remove noise low pass filter to noise

Graphical user interface

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Fig 5.3: Frequency response of second order low pass filter 1khz

# Peripheral setup

## Pin Mapping

|  |  |  |
| --- | --- | --- |
| Signal Name | Description | TI interface |
| PWM\_PFC\_1H\_P | Inductor 1 high side gate driver | P6 |
| PWM\_PFC\_1L\_P | Inductor 1 low side gate driver | P7 |
| PWM\_PFC\_4H\_P | Low frequency switch high side gate driver | P8 |
| PWM\_PFC\_4L\_P | Low frequency switch low side gate driver | P9 |
| PWM\_PFC\_3H\_P | Inductor 3 high side gate driver | P0 |
| PWM\_PFC\_3L\_P | Inductor 3 high side gate driver | P1 |
| PWM\_PFC\_2H\_P | Inductor 2 high side gate driver | P2 |
| PWM\_PFC\_2L\_P | Inductor 2 high side gate driver | P3 |
|  |  |  |
| PFC\_L4\_CS\_VREF | Inductor 2 current sense reference voltage | AA4 |
| PFC\_L3\_CS\_VREF | Inductor 3 current sense reference voltage | AB3 |
| PFC\_L5\_CS\_FILT\_DIG | Inductor 3 current sense | AA3 |
| PFC\_L4\_CS\_FILT\_DIG | Inductor 2 current sense | AB5 |
| PFC\_L3\_CS\_FILT\_DIG | Inductor 1 current sense | AA5 |
| HV\_PFC\_SENSE\_DIG | DC bus voltage sensing | AB4 |
| P277VAC\_IN\_CURR\_SENSE\_FILT\_DIG | Input AC current sense | AB7 |
| P277VAC\_IN\_CURR\_SENSE\_VREF\_DIG | Input AC current sense reference voltage | AA0 |
| PFC\_L5\_CS\_VREF\_DIG | Inductor 3 current sense reference voltage | AB2 |
| TMP\_PFC\_PWR\_STAGE\_DIG | Power stage temperature sense. | AA2 |
| VAC\_SENSE\_N\_DIG | Input AC voltage positive cycle sense | AB1 |
| VAC\_SENSE\_P\_DIG | Input AC voltage negative cycle sense | AA7 |

## PWM

### High frequency bridge

#### Counting mode

Up counter

#### operating frequency

Operating frequency of 100 khz from a period length of 899

#### Duty Cycle

The duty cycle of the PWM is a control input and is driven by the output of the current controller to modulate current and subsequently voltage. The range of the duty cycle is period length 0 – 899, which represents 0 -100%

Graphical user interface, text, application, email

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Fig 6.1 : configuration of PWM frequency, mode and Duty cycle

#### phase shift

The three interleaved phases are to 120 degrees apart, this is done by synching the counter period of the three PWM outputs (ePWM1, ePWM2 and ePWM4) such that the two PWMs are 120 and 240 degrees out of phase with the leading one. This is done to minimize ripple in the output voltage of the PFC. The phase offset value which is dependent on the period length is set to determine the phase, hence a fraction of it.

Graphical user interface, text, application

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Fig 6.2(a) : configuration of reference PWM Fig 6.2(b): configuration of PWM with 120 degrees phase shift

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Fig6.2(c) :configuration of PWM with 240 dergees phase shift

#### dead band

The dead band between the high side and low side switch needs to be 10 clock cycles with the RED applied to the ePWMA and FED applied to ePWMB

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Fig 6.3: configuration of PWM with Phase shift

### Low Frequency bridge

#### Operating frequency

N/A

#### Counting mode

Up count

#### Duty Cycle

899 or 100%

#### PHASE shift

N/A

#### Dead band

10 clock cycles

## ADC (Analog to digital converter)

### Output DC bus voltage

Software Triggered measurement sampled at 10khz

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Fig 6.4 configuration DC bus voltage measurment ADC

### Inductor Current

PWM triggered measurement at 100khz sampled at the middle of the PWM counter by ePWM4

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Fig 6.5(a & b) configuration of ADC measurement and reference for inductor current

### Input AC voltage

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Description automatically generatedPWM triggered measurement at 100khz sampled at the middle of the PWM counter

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Fig 6.6 configuration of measurement of positive and negative half cycle of AC voltage

### Input AC current

Software triggered interrupt sampled at 1khz

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Fig 6.7a

# Software in the loop (sil)

The controller is simulated in Simulink with the plant model load at 50 ohms and the controller in continuous time

A picture containing graphical user interface

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Fig 7.1 : result of the software in the loop solution showing PFC output voltage, inductor current, input voltage, and PI current controller output respectively.

# APPENDIX

## Abbreviations

PWM – pulse width modulation

ADC – analog to digital converter

kHz – kilo hertz

DC- direct current

AC- alternating current

CCM- continuous conduction mode

PFC – power factor correction

FET – field effect transistor

MCU -microcontroller unit

RED – rising edge dead band

FED – falling edge dead band